

IN THE CLAIMS:

- 1-11. (Cancelled)
12. (Original) A semiconductor device comprising:
- a substrate;
  - a gate dielectric deposited on the substrate, wherein the gate dielectric is made of high dielectric permittivity material; and
  - a gate formed on top of a  $\text{Si}_{1-x}\text{Ge}_x$  first layer comprising:
    - a  $\text{Si}_{1-x}\text{Ge}_x$  first layer formed directly on the gate dielectric, where  $0.5 < x \leq 1$ ; and,
    - a  $\text{Si}_{1-y}\text{Ge}_y$  second layer, formed on top of the  $\text{Si}_{1-x}\text{Ge}_x$  first layer where  $0 \leq y \leq 1$ .
13. (Original) The semiconductor device of claim 12, wherein at least one of the  $\text{Si}_{1-x}\text{Ge}_x$  first layer and the  $\text{Si}_{1-y}\text{Ge}_y$  second layer is predominantly Ge.
14. (Currently Amended) The semiconductor device of claim 12, wherein the gate further comprises a layer for limiting ~~[[the]]~~ a diffusion of at least one of Ge and Si between the  $\text{Si}_{1-y}\text{Ge}_y$  second layer and the  $\text{Si}_{1-x}\text{Ge}_x$  first layer.
15. (Original) The semiconductor device of claim 12, wherein the gate dielectric is selected in a group of metal oxides consisting of  $\text{HfO}_2$ ,  $\text{ZrO}_2$ ,  $\text{HfSiO}$  and  $\text{ZrSiO}$ .
16. (Original) The semiconductor device of claim 12, wherein  $x=1$ .

17. (Original) The semiconductor device of claim 12, wherein  $x=y=1$ .
18. (Original) The semiconductor device of claim 12, wherein an interface between the gate dielectric and the gate is predominantly made of Si.